A screenshot of a computer

Description automatically generated with medium confidence

The final result is stored in register A and register B

16’b 1111 1110 1001 1101 in 2's complement representation = -413 in decimal

Second Half of the final result stored in register B

8’h63 = 8’ 1001 1101

First Half of the final result stored in register A

8’hFE = 8’b 1111 1110

ClearA\_LoadB is set to 0 to Clear register A and load S into register B since it’s an active-low signal

Execute is set to 0 to start the operation since it’s an active-low signal

Switches are set to 8’b 1100 0101

(-59 in decimal)

Switches are set to 8’b 0000 0111

(7 in decimal)

Switches are first set to 8’b 0000 0000

Reset is set to 1 to clear all the registers: register X, register A, and register B since it’s an active-high signal